B.E. Semester-III (E.C.) Question Bank

(Digital Electronics)

All questions carry equal marks (10 marks)

Q.1	**Do as directed:**		
	1.	$(516)_7 = (\quad)_{10} = (\quad)_{16}$	
	2.	$(250.5)_{10} = (\quad)_8 = (\quad)_4$	
	3.	$(2ED)_{16} = (\quad)_8 = (\quad)_2$	
	4.	$(38)_9 = (\quad)_5 = (\quad)_2$	
	5.	Obtain the 9's and 10's complement of $(864)_{10}$.	
Q.2	**Do as directed:**		
	1.	$(198)_{12} + (12121)_3 = (\quad)_8$	
	2.	Determine the value of base x if $(50)_x = (203)_4$	
	3.	Given the two binary numbers X = 1010101 and Y = 1001011, perform the subtraction X-Y using 1's complements.	
	4.	Using 10's complement perform $(4572)_{10} - (2102)_{10}$.	
	5.	Multiply the $(135)_6$ and $(43)_6$ in the given base without converting to decimal.	
Q.3	**Do as directed:**		
	1.	$(347)_{10} = (\quad)_2 = (\quad)_8 = (\quad)_5 = (\quad)_{16} = (\quad)_{BCD}$	
	2.	$(11010111.110)_2 = (\quad)_{10} = (\quad)_{12} = (\quad)_{16}$	
	3.	Obtain the 9's and 10's complement of $(389.61)_{10}$.	
Q-4	**Do as directed:**		
	1.	Multiply the $(267)_8$ and $(71)_8$ in the given base without converting to decimal.	
	2.	$(103)_4 + (50)_7 = (\quad)_9$	
	3.	Determine the value of base b if $(211)_b = (152)_8$	
	4.	Given the two binary numbers X = 11010 and Y = 1101, perform the subtraction X-Y using 2's complement.	
	5.	Using 9's complement perform $(582)_{10} - (1002)_{10}$.	
Q.5	**(a)**	Define duality principal and explain it with the help of example. Find the complements of the functions **F1 = x'yz' + x'y'z** and **F2 = x(y'z'+yz)** by taking their duals and complementing each literal.	
	(b)	Demonstrate by means of truth tables the validity of the De Morgan's theorems for three variables. Find the complement of **F = a(b'c'+bc)** by applying De Morgan's theorem as many times as necessary.	
Q.6	**(a)**	Demonstrate by means of truth table the validity of the distributive law of **+** over **·**. Also show that the NOR and NAND operators are not associative.	
	(b)	Prove that a positive-logic AND gate is a negative-logic OR gate and vice-versa.	
Q.7	**(a)**	Express the Boolean function **F(p, q, r, s)=s(p'+q)+q's** in a sum of minterms and a product of maxterms.	
	(b)	Given the Boolean function: **F=xy+x'y'+y'z**	
		1.	Implement it with *only* OR and NOT gates.
		2.	Implement it with *only* AND and NOT gates.
Q.8	**(a)**	What is the difference between canonical form and standard form? Express the Boolean function **F(p, q, r)=(pq+r)(q+pr)** in a sum of minterms and a product of maxterms.	
	(b)	Realize 2 input X-OR gate using NOR gates only.	
Q.9	**(a)**	Simplify the following Boolean expressions by manipulation of Boolean algebra.	
		1.	F(x,y,z)=xy+xyz+xyz'+x'yz
		2.	F(A,B,C,D)=A'C(A'BD)'+A'BC'D'+AB'C

	(b)	Simplify the Boolean function $\mathbf{F(w,x,y,z)=w'x'z'+w'yz+w'xy}$ using don't care conditions $\mathbf{d=w'xy'z+wyz+wx'z'}$ in (i) sum of products and (ii) product of sums using Karnaugh map.
Q.10	**(a)**	Prove that:
		1. $wx+x'y+wy=wx+x'y$
		2. $(AB+C+D)(C'+D)(C'+D+E)=ABC'+D$
		3. $(A+B)'(A'+B')'=0$
	(b)	Simplify the function $F(A,B,C,D,E)=\Sigma m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$ using Karnaugh map.
Q.11	**(a)**	Reduce the following Boolean expressions to the required number of literals.
		1. $F(A,B,C,D)=(A+C+D)(A+C+D')(A+C'+D)(A+B')$ to four literals.
		2. $F(w,x,y,z) = [(yz)'+w]'+w+yz+wx$ to three literals
	(b)	Simplify the Boolean functions $F= w'(x'y + x'y'+ xyz) +x'z' (y+w)$ using don't-care conditions $d=w'x (y'z + yz') + wyz$ in (i) sum of products and (ii) product of sums using Karnaugh map.
Q.12	**(a)**	Simplify the following Boolean expressions.
		1. $F(w,x,y,z) = xy+wy'+wx+xyz$
		2. $F(p, q, r, s) = (p'+q) (p+q+s)s'$
	(b)	Simplify the following Boolean functions using Karnaugh map:
		1. $F(A,B,C,D)=\Pi(0,1,2,3,4,10,11)$
		2. $F(w,x,y,z)=\Sigma m(0,1,2,4,5,12,13,14)$ + don't care conditions $\Sigma d(6,8,9)$.
Q.13	**Write brief notes on:**	
	(a)	Full adder
	(b)	Read-Only Memory (ROM)
Q-14	**(a)**	Why are NAND and NOR gates known as universal gates? Explain in detail.
	(b)	Explain full- subtractor. Implement a full-subtractor with two half- subtractors and an OR gate.
Q.15	Implement Boolean functions	
	(a)	$F= (A +B') (CD+E)$ using only NAND gates.
	(b)	$F=A (B+CD) +BC'$ with only NOR gates.
	(c)	$F=x'y+xy'$ using only four NAND gates.
Q.16	Simplify the function $F(w,x,y,z)=\Sigma(0,1,2,8,10,11,14,15)$ using tabulation method.	
Q.17	Using the tabulation method, obtain the simplified expression in product of sums for the Boolean function $F(w,x,y,z)=\Pi(1,3,5,7,13,15)$.	
Q.18	Simplify the Boolean function $F(A,B,C,D,E,F)=\Sigma(6,9,13,18,19,25,27,29,41,45,57,61)$ using tabulation method.	
Q.19	**Write short notes on:**	
	(a)	Design of BCD-to-excess-3 code converter
	(b)	Programmable Logic Array (PLA)
Q.20	Differentiate between combinational logic circuit and sequential logic circuit. Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.	
Q.21	Design a combinational circuit whose input is a four-bit number and whose output is the 2's complement of the input number.	
Q.22	Design a combinational circuit that converts a decimal digit from the 2,4,2,1 code to the 8,4,-2,-1 code.	
Q.23	Design a combinational circuit that multiplies by 5 an input decimal digit represented in BCD. The output is also in BCD. Show that the output can be obtained from the input lines without using any logic gates.	
Q.24	Design a combinational circuit that converts a four-bit reflected-code number to a four-bit binary number. Implement the circuit with exclusive-OR gates.	

Q.25	Write note on "Binary parallel adder". Also draw logic diagram of a look-ahead carry generator and describe 4-bit full adder with look-ahead carry in detail.	
Q.26	**(a)**	Construct BCD adder using two 4-bit binary parallel adder and logic gates.
	(b)	Explain 4-bit magnitude comparator.
Q.27	Describe decoders using suitable example and design a BCD-to-decimal decoder.	
Q.28	Describe digital multiplexer in detail using suitable example. Obtain an 8×1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines. Use block diagram construction.	
Q.29	**(a)**	Construct a 5 × 32 decoder with four 3 × 8 decoder and a 2 × 4 decoder. Use block diagram construction only.
	(b)	Implement Boolean function $F(A,B,C,D)=\Sigma m(0,1,3,4,8,9,15)$ using 8:1 multiplexer.
Q.30	**(a)**	Design 3-bit binary counter using T flip-flop.
	(b)	Discuss "Digital IC logic families and characteristic of basic gate in each family".
Q.31	Explain race-around condition in relation to the J-K flip-flops using timing relationships. Draw the clocked Master-Slave J-K flip-flop configuration and explain how it removes race-around condition in J-K flip-flops.	
Q.32	Describe triggering of flip-flops and explain operation of an edge triggered D flip-flop.	
Q.33	Write state equations for all flip-flops. Design a sequential circuit with JK flip-flops to satisfy the following state equations: A(t+1)=A'B'CD+A'B'C+ACD+AC'D' B(t+1)=A'C+CD'+ A'BC' C(t+1)=B D(t+1)=D'	
Q.34	Draw the logic diagram of clocked RS Flip-Flop and explain its operation. Design a counter with the following binary sequence: 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use RS flip-flops.	
Q.35	Explain 4-bit synchronous up-down binary counter.	
Q.36	Describe shift registers and explain 4-bit bidirectional shift register with parallel load.	
Q.37	Differentiate between synchronous counter and ripple counter. Explain BCD ripple counter with logic diagram and timing diagram.	
Q.38	**Write Short notes on:**	
	1. Complementary MOS (CMOS) 2. BCD synchronous counter	
Q.39	**Write Short notes on:**	
	1. Emitter-coupled Logic (ECL) 2. Ring counter	
Q.40	**Write Short notes on:**	
	1. Schottky TTL gate 2. 4-bit binary ripple counter	
